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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	10/022,297	MORITA ET AL.
	Examiner	Art Unit
	Monica Lewis	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-16 and 18-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-16 and 18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *18 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed June 13, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 4-16 and 18-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 1, 4 and 8 are objected to because of the following informalities: a) the way the claim is written it seems like the resin covers only the land and not the solder and chip. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 5-12 are rejected under 35 U.S.C. 103(a) as obvious over Sakamoto (U.S. Patent No. 6,259,157).

In regards to claim 1, Sakamoto et al. ("Sakamoto") discloses the following:

a) a substrate (1), a land (6 and 7) formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin covering the land, the solder layer and the semiconductor chip on the substrate (For Example: See Figure 1 and Column 6 Lines 25-29).

In regards to claim 1, Sakamoto fails to disclose the following:

a) a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the land.

Although Sakamoto fails to specifically disclose the limitations listed above, the same material is utilized in Sakamoto as in Applicant's invention therefore it would have the same characteristics.

In regards to claim 4, Sakamoto discloses the following:

a) a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin covering the land, the solder layer and the semiconductor chip on the substrate (For Example: See Figure 1 and Column 6 Lines 18-29).

In regards to claims 4 and 12, Sakamoto fails to disclose the following:

a) a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of aluminum.

Although Sakamoto fails to specifically disclose the limitations listed above, the same material is utilized in Sakamoto as in Applicant's invention therefore it would have the same characteristics.

In regards to claim 5, Sakamoto fails to disclose the following:

a) the coefficient of the expansion of the synthetic resin is generally less than approximately 23 ppm/K.

Although Sakamoto fails to specifically disclose the limitations listed above, the same material is utilized in Sakamoto as in Applicant's invention therefore it would have the same characteristics.

In regards to claim 6, Sakamoto discloses the following:

a) land comprises copper (For Example: See Column 6 Lines 25-29).

In regards to claim 7, Sakamoto discloses the following:

a) synthetic resin includes epoxide (For Example: See Figure 1).

In regards to claim 8, Sakamoto discloses the following:

a) a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin covering the land, the solder layer and the semiconductor chip on the substrate (For Example: See Figure 1 and Column 6 Lines 18-29).

In regards to claim 8, Sakamoto fails to disclose the following:

a) a coefficient of expansion of the synthetic resin being generally less than a larger one of a coefficient of expansion of the substrate and a coefficient of expansion of the land, and the coefficient of expansion of the resin being generally greater than a smaller one of the coefficient of expansion of the land.

Although Sakamoto fails to specifically disclose the limitations listed above, the same material is utilized in Sakamoto as in Applicant's invention therefore it would have the same characteristics.

In regards to claim 9, Sakamoto fails to disclose the following:

a) a coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the substrate and is greater than the a coefficient of expansion of the land.

Although Sakamoto fails to specifically disclose the limitations listed above, the same material is utilized in Sakamoto as in Applicant's invention therefore it would have the same characteristics.

In regards to claim 10, Sakamoto fails to disclose the following:

a) a coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the land and is greater than the a coefficient of expansion of the substrate.

Although Sakamoto fails to specifically disclose the limitations listed above, the same material is utilized in Sakamoto as in Applicant's invention therefore it would have the same characteristics.

In regards to claim 11, Sakamoto discloses the following:

a) substrate comprises aluminum (For Example: See Column 6 Line 18).

6. Claim 13 is rejected under 35 U.S.C. 103(a) as obvious over Sakamoto (U.S. Patent No. 6,259,157) in view of Ueda (Japanese Publication No. 08-264674).

In regards to claim 13, Sakamoto discloses the following:

a) the semiconductor chip defines at least two corners positioned generally opposite to each other, the land has an outer boundary that defines at least two corner portions in proximity to the corners of the semiconductor chip (For Example: See Figure 1).

In regards to claim 13, Sakamoto fails to disclose the following:

a) the outer boundary further defines contiguous portions extending next to the corner portions and spaced apart from the semiconductor chip more than the corner portions, and the corner portions of the land generally confine the corners of the semiconductor chip therein.

However, Ueda discloses a land (For Example: See Figure 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sakamoto to include a land as disclosed in Ueda because it aids in keeping the chip from coming off of the substrate (For Example: See Abstract).

Additionally, since Sakamoto and Ueda are both from the same field of endeavor, the purpose disclosed by Ueda would have been recognized in the pertinent art of Sakamoto.

7. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as obvious over Sakamoto (U.S. Patent No. 6,259,157) in view of Yamanashi (Japanese Patent No. JP02000253570A).

In regards to claim 14, Sakamoto fails to disclose the following:

a) the semiconductor chip controls electric power.

However, Yamanashi discloses a chip that controls power (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sakamoto to include a chip that controls power as disclosed in Yamanashi because it aids in preventing damages to the motor controller (For Example: See Abstract).

Additionally, since Sakamoto and Yamanashi are both from the same field of endeavor, the purpose disclosed by Yamanashi would have been recognized in the pertinent art of Sakamoto.

In regards to claim 15, Sakamoto fails to disclose the following:

a) the semiconductor chip controls power of an electric motor arranged to drive an electric vehicle.

However, Yamanashi discloses a chip that controls power (For Example: See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Sakamoto to include a chip that controls power as disclosed in Yamanashi because it aids in preventing damages to the motor controller (For Example: See Abstract).

Additionally, since Sakamoto and Yamanashi are both from the same field of endeavor, the purpose disclosed by Yamanashi would have been recognized in the pertinent art of Sakamoto.

8. Claims 16, 18, 19, 21, 23, 24 and 26 are rejected under 35 U.S.C. 103(a) as obvious over Ueda (Japanese Publication No. 08-264674) in view of Yanagisawa (Japanese Patent No. 63213936).

In regards to claim 16, Ueda et al. ("Ueda") discloses the following:

a) a substrate (3), a land (10) formed on the substrate, a semiconductor chip (1) mounted on the land, the semiconductor chip defining at least two corners positioned generally opposite to each other, the land having an outer boundary defining at least two corner portions disposed in proximity to the corners of the semiconductor chip, the outer boundary defining contiguous potions extending next to the corner portions and spaced apart from the semiconductor chip more than the corner portions, the corner portions of the land generally confining the corners of the semiconductor chip (For Example: See Figure 3).

In regards to claim 16, Ueda fails to disclose the following:

a) a solder layer joining the semiconductor chip with the land.

However, Yanagisawa discloses a solder layer (For Example: See Figure 2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ueda to include a solder layer as disclosed in Yanagisawa because it aids in bonding elements together (For Example: See Abstract).

Additionally, since Ueda and Yanagisawa are both from the same field of endeavor, the purpose disclosed by Yanagisawa would have been recognized in the pertinent art of Ueda.

In regards to claim 18, Ueda discloses the following:

a) the semiconductor chip is generally configured as a shape having at least one diagonal line, and the corners of the semiconductor chip are positioned on the diagonal line of the shape (For Example: See Figure 3).

In regards to claim 19, Ueda discloses the following:

a) the semiconductor chip defines four corners, and the land defines four corner portions corresponding to the corners of the semiconductor chip (For Example: See Figure 3).

In regards to claim 21, Ueda discloses the following:

a) land is generally configured as a rectangular shape except for the corner portions (For Example: See Figure 3).

In regards to claim 23, Ueda discloses the following:

a) area of the land is larger than an area of the semiconductor chip, and the area of the land generally shrinks toward the corners of the semiconductor chip (For Example: See Figure 3).

In regards to claim 24, Ueda discloses the following:

a) area of the land is larger than an area of the semiconductor chip, and the area of the land generally expands from the corners of the semiconductor chip (For Example: See Figure 3).

In regards to claim 26, Ueda fails to disclose the following:

a) semiconductor chip is joined with the land in a reflow soldering method.

However, the limitation of "reflow soldering method" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*,

218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as obvious over Ueda (Japanese Publication No. 08-264674) in view of Yanagisawa (Japanese Patent No. 63213936) and Ohuchi (U.S. Patent No. 6,181,003).

In regards to claim 20, Ueda discloses the following:

a) the semiconductor chip is generally configured as a rectangular shape (For Example: See Figure 3).

In regards to claim 20, Ueda fails to disclose the following:

a) at least a length of a shorter side of the rectangular shape is longer than approximately 2.5 millimeters.

However, Ohuchi discloses sides that are longer than 2.5 mm (For Example: See Column 5 Lines 12-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ueda to include sides longer than 2.5 mm as disclosed in Ohuchi because it aids in improving reliability (For Example: See Abstract and Column 1 Lines 5-16)).

Additionally, since Ueda and Ohuchi are both from the same field of endeavor, the purpose disclosed by Ohuchi would have been recognized in the pertinent art of Ueda.

Finally, the applicant has not established the critical nature of the dimension of 2.5 millimeters. "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a

situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

10. Claim 22 is rejected under 35 U.S.C. 103(a) as obvious over Ueda (Japanese Publication No. 08-264674) in view of Yanagisawa (Japanese Patent No. 63213936) and Tani (U.S. Patent No. 5,468,993).

In regards to claim 22, Ueda fails to disclose the following:

a) a round shape except for the corner portions.

However, Tani discloses a round shape pad (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ueda to include a round shape pad as disclosed in Tani because it aids in preventing short circuit (For Example: See Column 1 Lines 9-16).

Additionally, since Ueda and Tani are both from the same field of endeavor, the purpose disclosed by Tani would have been recognized in the pertinent art of Ueda.

11. Claim 25 is rejected under 35 U.S.C. 103(a) as obvious over Ueda (Japanese Publication No. 08-264674) in view of Yanagisawa (Japanese Patent No. 63213936) and Yamanashi (Japanese Patent No. JP02000253570A).

In regards to claim 25, Ueda fails to disclose the following:

a) the semiconductor chip controls electric power.

However, Yamanashi discloses a chip that controls power (See Abstract). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify

the semiconductor device of Ueda to include a chip that controls power as disclosed in Yamanashi because it aids in preventing damages to the motor controller (See Abstract).

Additionally, since Yanagisawa and Yamanashi are both from the same field of endeavor, the purpose disclosed by Yamanashi would have been recognized in the pertinent art of Yanagisawa.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
September 3, 2003

AMIR ZARABIAN
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